Abstract of the Disclosure

P-wells (21) are formed in, for example, a matrix in an N-type semiconductor layer (20). At an outer periphery of each of the P-wells (21) is formed, for example, a rectangular ring-shaped N^+-type diffused source region (22), between which and an N-type semiconductor layer (20) which provides a drain region (23) is formed a channel region (26). A source electrode (33) is formed in such a manner as to be contact with the center portion of each of the P-wells (21) and the source region (22) in such a construction that a contact portion (40) of the P-well with the source electrode consists of P^+-type regions and N^+-type regions formed alternately. As a result, it is possible to rapidly eliminate the minority carrier generated in the P-well owing to a counter electromotive force etc., thus speeding the switching operations.